

Design and Construction of the Digital Interruption Counter

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ABSTRACT

Nowadays the electronic digital interruption counter is very popular. It counts and records automatically the number of objects passing on a conveyor belt or the people entering or leaving any place through a particular gate. The interruption of light beam in this circuit is counted in three digits up to 999. The digital interruption counter circuit is constructed by using locally available electronic components. The circuit is very simple and construct with TTL integrated circuits.

Key Words: 7490 Decade counter IC, Seven segment decoder / driver IC 7447, Common-anode LED seven-segment display, Light Dependent Resistor (LDR), 555Timer IC, Power Supply.

1. INTRODUCTION

Digital Interruption Counter can be used at home or in business for counting and security applications. It senses the interruption of light falling on a Light Dependent Resistor (LDR), and advances a three digit common anode seven segment LED display one count with each interruption. If you want to know how many people or things pass a certain point, a counter is used. Counters are used on production lines, at public events, and at store entrances, among other applications.

Traditional electric and mechanical counters are triggered by switches located in places such as an mats or turnstiles [1]. The switches operate solenoids to advance the digits on the linked rotating drums. Because both mechanical and electric counters are essentially mechanical in operation, they are noisy, subject to failure from wear, and limited in their counting speed. True electronic counters, on the other hand, are completely silent and have no moving parts to wear out. They use lighted digits to display the count, and can operate at high speed. While some electronic counters use switches to trigger their counting, the interruption counter described in this research paper uses light as its count trigger. This digital interruption counter has a 3-common anode seven-segment LED display that counts to 999 before resetting 000. It uses seven integrated circuits to detect and count the interruption of light on a LDR, and shows the total count on three red LED seven-segment digital displays. It is completely silent, has no moving parts and can count at very high speed. The block diagram for this construction is shown in Figure 1.

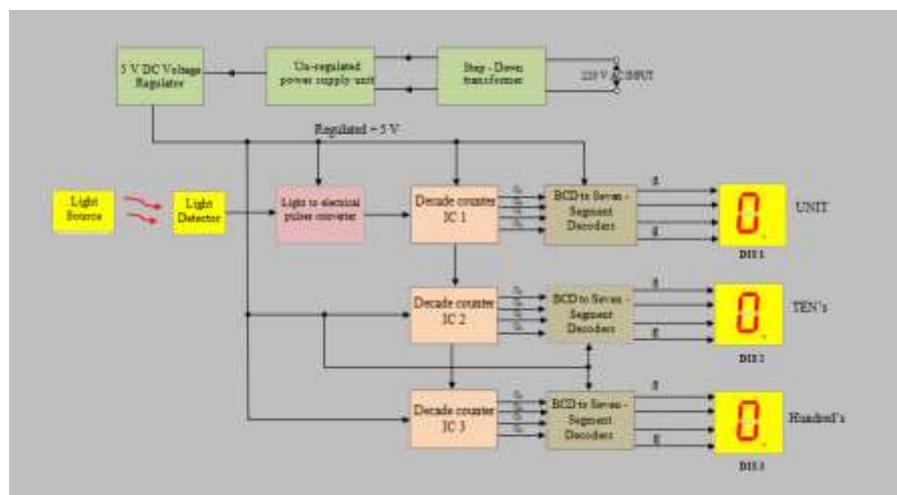


Figure 1. Block diagram of the Digital Interruption Counter

2. Background Theory

2.1 Photo Resistor

Photo resistors, also known as light dependent resistors (LDR), are light sensitive devices most often used to indicate the presence or absence of light, or to measure the light intensity. In the dark, their resistance is very high, sometimes up to $1M\Omega$, but when the LDR sensor is exposed to light, the resistance drops dramatically, even down to a few ohms, depending on the light intensity. LDRs have a sensitivity that varies with the wavelength of the light applied and are nonlinear devices [2].

2.2 Potential Divider Circuit with LDR

A *light-dependent resistor* (LDR) is a light sensitive resistor based on CdS photoconductive technology, which connects in a voltage divider configuration for proper biasing. Most input sensor (LDR) varies their resistance and usually a voltage divider is used to convert this to a varying voltage which is more useful. The voltage signal can be fed to other parts of the circuit, such as the input to an IC or a transistor switch. The value of the resistor R will determine the range of the output voltage V_o [4].

2.3. 555 Timer IC

The 555 timer IC is a very cheap, popular and useful precision timing device which can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing a string of stabilised waveforms of varying duty cycles from 50 to 100%. The single 555 Timer chip in its basic form is a Bipolar 8-pin mini Dual-in-line Package (DIP) device consisting of some 25 transistors, 2 diodes and about 16 resistors arranged to form two comparators, a flip-flop and a high current output stage [2, 5].

2.4 Monostable Multivibrator Using 555 Timer

Monostable Multivibrator is also known as One Shot Multivibrator. As its name indicates it has one stable state and it switches to unstable state for a predetermined time period T when it is triggered. The time period T is determined by the RC time constant in the circuit. Monostable multivibrator using 555 timer IC. In this circuit, 8th pin and 1st pin of the 555 timer are used to given power V_{cc} and Ground respectively. 4th pin is the Reset pin of 555 Timer, which is active low so it is connected to V_{cc} to avoid accidental resets. 5th pin is the Control Voltage pin used to provide external reference voltage to internal comparators. Since it is not used here, it is grounded via a capacitor C' ($0.01\mu F$) to avoid high frequency noises. When a negative trigger is applied on the Trigger input of 555, output goes high and capacitor starts charging through resistor R. When the capacitor voltage becomes greater than $2/3 V_{cc}$, output goes low and capacitor starts discharging through the discharge pin of 555 Timer. Time period of the unstable state is given by $T = 1.1RC$ [2,5].

2.5 J-K Flip-Flop

The J-K flip-flop is very similar to the other clocked flip-flops, although certain differences exist that make the J-K special. When \overline{J} and K are both 0 the flip-flop is inhibited, Q is the same after the CK pulse as it was before; there is no change at the output. If J and K are at different logic levels, then after the CK pulse, Q and \overline{Q} will take up the same states as J and K. For example, if $J = 1$ and $K = 0$, then on the trailing (negative going) edge of a clock pulse, the Q output will be set to 1, and if $K = 1$ and $J = 0$ then the Q output is reset to logic 0 on the trailing edge of a clock pulse. If logic 1 is applied to both J and K, the output toggles at the trailing edge of each clock pulse, just like a toggle flip-flop. The JK flip-flop can therefore be called a 'programmable flip-flop' because of the way its action can be programmed by the states of J and K. Each of the above actions are synchronised with the clock pulse, data being taken into the master flip-flop at the rising edge of the clock pulse, and output from the slave flip-flop appears at the falling edge of the clock pulse [5, 6].

2.6 Decade Counter (BCD Counter)

A decade counter operates in the base - 10, or decimal, number system. The most significant bit of decade counter produces one output pulse for every 10 input pulses. The decimal counter forms the basis for digital event, period and frequency counter instruments. The decade counter shown in figure 7 is connected so that all four *clear* inputs are tied together to form a common clear line. This line is connected to the output of a TTL NAND gate, which is one section of a 7400 IC device. The rules of operation for the TTL NAND gate: If either input is LOW, then the output goes HIGH, but if both inputs are HIGH, then the output goes LOW. The output of the NAND gate will keep the clear line HIGH for all counts through 10. Counting operation of a decade counter using J-K Flip-Flops is shown in Table 2. It represents the count of circuit for decimal count of input pulses. The NAND gate output is zero when the count reaches 10 (1010). The count is decoded by the inputs of NAND gate B and D. After count 10, the logic gate NAND will trigger its output from 1 to 0, and it resets all flip flops [7, 8].

2.7 The 74LS90 BCD Counter

The 74LS90 integrated circuit is basically a MOD-10 decade counter that produces a BCD output code. The 74LS90 consists of four master-slave JK flip-flops internally connected to provide a MOD-2 (count-to-2) counter and a MOD-5 (count-to-5) counter. The 74LS90 has one independent toggle JK flip-flop driven by the CLK A input and three toggle JK flip-flops that form an asynchronous counter driven by the CLK B input as shown in figure 9. The counter's four outputs are designated by the letter symbol Q with a numeric subscript equal to the binary weight of the corresponding bit in the BCD counter circuit's code. The 74LS90 counting sequence is triggered on the negative going edge of the clock signal, that is when the clock signal CLK goes from logic 1 (HIGH) to logic 0 (LOW). The additional input pins R₁ and R₂ are counter "reset" pins while inputs S₁ and S₂ are "set" pins. When connected to logic 1, the Reset inputs R₁ and R₂ reset the counter back to zero, 0 (0000), and when the Set inputs S₁ and S₂ are connected to logic 1, they Set the counter to maximum, or 9 (1001) regardless of the actual count number or position. The 74LS90 counter consists of a divide-by-2 counter and a divide-by-5 counter within the same package. Then we can use either counter to produce a divide-by-2 frequency counter only, a divide-by-5 frequency counter only or the two together to produce our desired divide-by-10 BCD counter [7, 8].

2.8 Basic LED Seven-Segment Display Driver System

The block diagram of a basic LED seven segment display system that can display a given input in numerical form is shown in Figure 2 [5, 6].

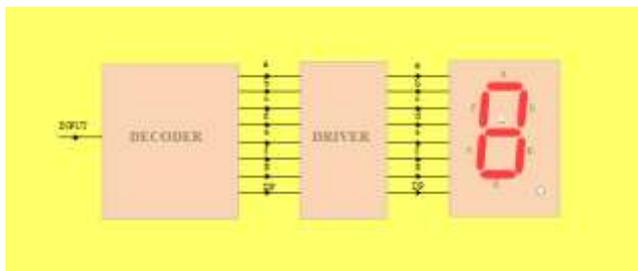


Figure 2. Basic 7 - segment LED display driver system.

2.9 Decoder/Driver IC 74LS47

Decoder/driver ICs are available in both TTL and CMOS forms. Some of these devices have integral ripple-blanking facilities, others have built-in data latches, and a few even have built-in decade counter stages, etc. The 74LS47 seven-segment decoder/driver IC is a member of the LS TTL family. Typical 74LS47 seven-segment decoder/driver IC is shown in Figure 12. It has integral ripple-blanking facilities, but does not incorporate data latches. A 74LS47 IC has three input 'control' terminals, these being designated LT (Lamp Test), BI/RBO, and RBI. The LT terminal drives all display outputs on when the terminal is driven to logic 0 with the RBO terminal open or at logic 1. When the BI/RBO terminal is pulled low, all outputs are blanked; this pin also functions as a ripple-blanking output terminal [2, 3].

3. Design and Operation of the Digital Interruption Counter

The digital interruption counter circuit is composed of five stages, namely power supply unit, light sensor and detector unit, light pulses to electrical pulses converter unit, BCD to decimal decoder unit and display unit. The complete schematic diagram of this circuit is shown in figure 3.

The dc power supply unit is an essential component of many electronics systems. The ac line input voltage 220 V is transformed to 12 V_{ac} by using a 12V-0-12V step-down transformer. The step-down voltage is applied to the bridge rectifier circuit to rectify the step-down voltage which produces the full-wave rectified output. The 1000µF/50V capacitor is sufficient to filter the ripple voltage according to its charging, discharging actions. The unregulated dc voltage is achieved from the capacitor filter which is regulated to have a regulated 5V, dc voltage by using a three-terminal positive voltage regulator IC, AN 7805. The regulated 5V, dc voltage is supplied to the digital interruption counter circuit.

The output of the regulator IC 7805 is connected to a 100 nF ceramic capacitor for filtering the noise voltage and it is also called a noise filter. The light sensor and detector unit of this circuit uses a Light Dependent Resistor (LDR) and a 470KΩ potentiometer. The voltage across the LDR depends on the light intensity. The output voltage of the LDR is connected to the base of an NPN transistor, C1815. When light falls on the LDR, its resistance is low. The total base voltage of the C1815 transistor is approximately equal to 0.56 volt which is less than 0.7 volt. This voltage is less than that required for the transistor to conduct and it goes into the cut-off region. Thus it doesn't conduct and the collector of this transistor is high.

Now, when any object is placed between the light source and LDR, the light falling on the LDR is interrupted and its resistance increases. The base voltage of C1815 becomes approx. 1.1 volts which is enough for the transistor to operate in saturation region. Thus it conducts and provides allow (0 V) output. The output voltage of the transistor (C1815) is fed to the light pulses to electrical pulses converter unit. So the objects to be counted are arranged in a row to move one by one in between the light source and light dependent resistor (LDR). The light pulses to electrical pulses converter stage consists of a 555 timer IC whose main function is to give electrical pulses when light pulses fall on the LDR. Each time the beam is interrupted, a pulse is produced. The LDR can detect interruptions even a few microseconds apart. These pulses are counted by three decade chain counters using 7490 ICs. Input is given to pin 14 of IC1 and output from pin 11 of this IC is fed to pin 14 of IC 2. IC 3 is similarly fed from IC 2.

A reset circuit is also used to reset the count to zero. For this SPDT switch, S1 is used whose one end is connected to + 5 V supply and another end is grounded. The output of this RESET switch S1 is connected to pin 2& 3 of each decade counter IC (IC2 through IC4). When the S1 is pressed, the digital interruption counter is reach to reset position and then 000 is appeared on the 7-segment display. In the decade counter IC 7490, the B input, pin (1) is connected to the Q_A output, pin (12). The input count pulses are applied to input A (pin 14). A symmetrical divide-by-ten count can be obtained from the 7490 counter by connecting the Q_D output (pin 11) to the A input (pin 14) and applying the input count be the B input (pin 1) which gives a divide-by-ten square wave at output Q_A (pin 12).

The contents of each decade counter are taken in BCD (binary coded decimal) form fed through IC 7447 BCD to 7- segment decoder driver and displayed on the corresponding common anode LED display. Thus the contents of IC2, IC3 and IC4 are displayed on DS1 (UNITS), DS2 (TENS), and DS3 (HUNDREDS) respectively.

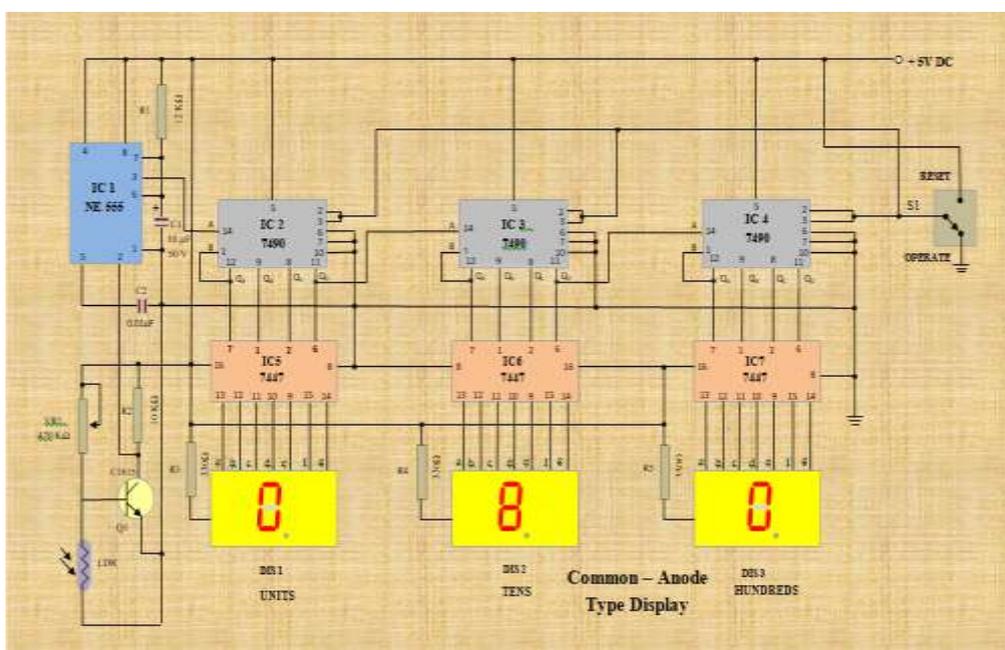


Figure 3. Complete schematic diagram of the digital interruption counter

The decoder/driver IC 7447 is used to change a coded input such as BCD to another code, decimal display. Inputs are A, B, C, D and the seven outputs a to g are meant to be connected to a seven - segment LED display. A common anode display has to be used with the 7447. The current limiting resistors are important, too. With only the LED connected, current could become excessive as the LED conducts. Typical current limit resistance is 270 Ω to 330 Ω. If inputs D C B A are 0 0 0 1, which is the BCD code for 1, only segments b and c light. Segments b and c form a single vertical line and give the appearance of a numeral 1. The counter circuit thus counts the number of times any object is passed between the light source and LDR. This circuit can count up to a maximum value of 999. Output data measurement of the digital interruption counter circuit is shown in Table 1.

Table 1. Output Data Measurement of the Digital interruption Counter

Table 1.1 Reset Condition of Decimal Counting Unit

IC 2 (74LS 90) UNITS COUNTER						IC 3 (74LS 90) TENS COUNTER						IC 4 (74LS 90) HUNDREDS COUNTER					
Pin2	Pin 3	Pin 11 Q _b	Pin 8 Q _c	Pin 9 Q _a	Pin 12 Q _λ	Pin2	Pin 3	Pin 11 Q _b	Pin 8 Q _c	Pin 9 Q _a	Pin 12 Q _λ	Pin2	Pin 3	Pin 11 Q _b	Pin 8 Q _c	Pin 9 Q _a	Pin 12 Q _λ
1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0

Decoder/Driver Unit

IC 5 (74LS 47) UNITS DECODER OUTPUT							IC 6 (74LS 47) TENS DECODER OUTPUT							IC 7 (74LS 47) HUNDREDS DECODER OUTPUT							
Pin 13 a	Pin 12 b	Pin 11 c	Pin 10 d	Pin 9 e	Pin 15 f	Pin 14 g	Pin 13 a	Pin 12 b	Pin 11 c	Pin 10 d	Pin 9 e	Pin 15 f	Pin 14 g	Pin 13 a	Pin 12 b	Pin 11 c	Pin 10 d	Pin 9 e	Pin 15 f	Pin 14 g	
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Display Unit

HUNDREDS DISPLAY DS 3							TENS DISPLAY DS 2							UNITS DISPLAY DS 1							Appear no. on Display Unit		
a	b	c	d	e	f	g	a	b	c	d	e	f	g	a	b	c	d	e	f	g	DS 3	DS 2	DS 1
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0

Operating Condition of Decimal Counting Unit

IC 2 (74 LS 90) UNITS COUNTER							IC 3 (74 LS 90) TENS COUNTER				IC 4 (74 LS 90) HUNDREDS COUNTER										
Pin 14 CK	Pin 2	Pin 3	Pin 11 Q _b	Pin 8 Q _c	Pin 9 Q _b	Pin 12 Q _a	Pin 14 CK	Pin 2	Pin 3	Pin 11 Q _b	Pin 8 Q _c	Pin 9 Q _b	Pin 12 Q _a	Pin 14	Pin 2	Pin 3	Pin 11 Q _b	Pin 8 Q _c	Pin 9 Q _b	Pin 12 Q _a	
0	0	0	0	0	0	1	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	1	0	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	1	1	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	1	0	0	0	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	1	0	1	0	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	1	1	0	0	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	1	1	1	0	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	1	0	0	0	0	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	1	0	0	1	0	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	-	0	0	0	0	0	0	0

IC 2 (74 LS 90) UNITS COUNTER							IC 3 (74 LS 90) TENS COUNTER				IC 4 (74 LS 90) HUNDREDS COUNTER										
Pin 14 CK	Pin 2	Pin 3	Pin 11 Q _b	Pin 8 Q _c	Pin 9 Q _b	Pin 12 Q _a	Pin 14 CK	Pin 2	Pin 3	Pin 11 Q _b	Pin 8 Q _c	Pin 9 Q _b	Pin 12 Q _a	Pin 14	Pin 2	Pin 3	Pin 11 Q _b	Pin 8 Q _c	Pin 9 Q _b	Pin 12 Q _a	
0	0	0	0	0	0	1	0	0	0	0	0	0	1	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0	1	-	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0	0	1	0	0	0	1	-	0	0	1	0	0	0	1

Display Unit

HUNDREDS DISPLAY DS 3							TENS DISPLAY DS 2							UNITS DISPLAY DS 1							Appear no. on Display Unit		
a	b	c	d	e	f	g	a	b	c	d	e	f	g	a	b	c	d	e	f	g	DS 3	DS 2	DS 1
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	2
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	3
0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	4
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	5
0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	6
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	0	7

HUNDREDS DISPLAY DS 3							TENS DISPLAY DS 2							UNITS DISPLAY DS 1							Appear no. on Display Unit		
a	b	c	d	e	f	g	a	b	c	d	e	f	g	a	b	c	d	e	f	g	DS 3	DS 2	DS 1
0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	9	9
1	0	0	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0
0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	9	9	9

4. DISCUSSION AND CONCLUSION

In this research report, the digital interruption counter was constructed with locally available electronic components. This circuit can be built with a light dependent resistor (LDR), a 555 timer IC, three decade counter ICs SN7490, three BCD to decimal decoder / driver ICs SN 7447 and a few additional parts. The light sensor and detector unit of this interruption counter circuit used light dependent resistor (LDR) and preset. The voltage across the LDR depends on the light intensity. The 555 timer IC was used as light pulses to electrical pulses converter circuit.

Three decade counter ICs SN 7490 counts the pulses generated by the 555 timer IC and give the corresponding BCD output. Three 7447 decoder display the count through common-anode LED display. The outputs of the decoder are connected to the respective segments of common-anode displays through resistors. The resistors are absolutely essential to minimize the current drawn by each segment which in turn should be low to increase the life of the displays. The value of these resistors varies with supply voltage. Any other regulated power supply can also be used, provided it can supply +5V at over 500 mA (with good heat sinking the 7805 can supply 1 amp).

The constructed digital interruption counter circuit could be used for counting objects on a conveyor belt etc. For domestic purpose it could be used to count the number of guests entering or leaving a room. (Provided entrance and exist are separate). We conclude that the constructed digital interruption counter circuit can be used for object counting equipment. Device parameters and new design techniques can be found on the basis of this various circuit design based on this thesis report to study the various field. Photograph of this circuit simulation is shown in Figure 4.



Figure 4. Object is passing through between light source and light sensor and Reset condition of Photograph of the digital interruption counter simulation

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